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SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE		DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/712,482	HATTI ET AL.
	Examiner Jose M. Torres	Art Unit 2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-43 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
 5) Claim(s) ____ is/are allowed.
 6) Claim(s) 1-36 and 38-41 is/are rejected.
 7) Claim(s) 37, 42 and 43 is/are objected to.
 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 13 November 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

1. The Preliminary Amendment filed on March 15, 2004, have been entered and made of record.

Drawings

2. The drawings are objected to because:

- Reference Character 48C(0) in the second line of Frame Buffer 48C in Figure 3A should be -- 48C(1) --
- Reference Character for Multiplexer 1210 in Figure 10 is missing.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:
 - Page 15, Paragraph [0051] line 6: "via the video encoder" should be -- via the video encoder 55 --

Appropriate correction is required.

Claim Objections

4. Applicant is advised that should claim 36 be found allowable, claim 34 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim.

See MPEP § 706.03(k).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 17, 22, and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 17 recites the limitation "the byte order" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. However, it appears to be "the pixel order", and has been treated as such. Affirmation of this is required by the appropriate amendment.

Claim 22 recites the limitation "the byte order" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. However, it appears to be "the pixel order", and has been treated as such. Affirmation of this is required by the appropriate amendment.

Claim 26 recites the limitation "the state machine" in Page 35 line 6. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-14, 16-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mino et al. (US 6,927,776) in view of Childers et al. (US 5,838,955).

As to claims 1, 8, 16 and 21, Mino et al. teaches a method/system for displaying frames/pictures (Col. 6 lines 49-51), said method/system comprising: fetching (a first circuit for fetching) a portion of a frame stored in a frame buffer, the portion of the frame stored with a byte/pixel order (FIG. 1, “frame buffer region **22** and data transfer”, Col. 6 line 47 through Col. 7 line 8 and FIGs. 9C-D, Col. 9 lines 24-33); storing (a buffer for storing) the portion of the frame in another buffer with the byte/pixel order (FIG. 1, “data buffer **11**”, Col. 6 lines 12-19); fetching (a state machine/an input data write unit for fetching) a plurality of pixels from the portion of the frame (FIG. 1, “data processor **9**”, Col. 15 lines 11-25).

However, Mino et al. fails to disclose converting (a second circuit for converting) the byte order of the plurality of pixels to a predetermined byte order, the byte order being different from the predetermined byte/pixel order.

Childers et al. teach converting (a second circuit for converting) the byte order of the plurality of pixels to a predetermined byte order (“standard format”), the byte order being different from the predetermined byte/pixel order (FIG. 4B, “byte reordering logic **457**”, Col. 6 lines 35-40).

Therefore, in view of Childers et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mino et al.’s

method/system by incorporating the method step and the byte reordering logic for converting the byte order of the plurality of pixels to a predetermined byte order, the byte order being different from the predetermined byte order in order to write and read pixel data in a standard format regardless of the format in which a video input device creates it (Col. 6 lines 35-40).

As to claims 2, 9, 17 and 22 as understood, Mino et al. further teaches decoding (a video decoder for decoding) the frame (FIG. 1, “address decoder **12**”, Col. 5 lines 47-64 and Col. 6 lines 12-19); and storing (the frame buffer for storing) the frame with the byte order (FIG. 1, “main memory **2**”, Col. 6 line 14-19 and FIG. 9B, Col. 9 lines 19-23).

As to claims 3, 4, 11, 12, 18, 19, 23 and 24, Mino et al. further teaches the another buffer (the buffer) forms a portion of a display engine (FIG. 1, “interface section **10**” and a portion of a pixel feeder (FIG. 1, “transfer parameter generator **14**”, Col. 5 lines 38-46).

As to claims 5 and 13, Mino et al. fails to disclose the predetermined order is selected from a group consisting of big endian byte order and little endian byte order.

Childers et al. further teaches the predetermined order is selected from a group consisting of big endian byte order and little endian byte order (Col. 6 lines 35-40 and line 59 through Col. 7 line 8).

As to claim 6, Mino et al. fails to disclose providing an indicator indicating whether the byte order is different or opposite from the predetermined order.

Childers et al. further teaches providing an indicator indicating whether the byte order is different or opposite from the predetermined order (FIG. 4A, "ADDR INVARIANT MODE, byte swap multiplexors **449, 451**", Col. 6 line 59 through Col. 7 line 8).

As to claim 7, Mino et al. fails to disclose swapping a first one of the plurality of pixels and a second one of the plurality of pixels if the indicator indicates that the byte order is different or opposite from the predetermined order; and swapping a third one of the plurality of pixels and a fourth one of the plurality of pixels if the indicator indicates that the byte order is different or opposite from the predetermined order.

Childers et al. further teaches swapping a first one of the plurality of pixels and a second one of the plurality of pixels (FIG. 4A, output of multiplexor **449**) if the indicator (ADDR INVARIAN MDOE) indicates that the byte order is different or opposite from the predetermined order; and swapping a third one of the plurality of pixels and a fourth one of the plurality of pixels (FIG. 4A, output of multiplexor **451**) if the indicator (ADDR INVARIAN MODE) indicates that the byte order is different or opposite from the predetermined order (Col. 6 line 59 through Col. 7 line 8).

As to claim 10, Mino et al. further teaches the first circuit comprises an input data write unit (FIG. 1, "data processor **9**", Col. 15 lines 11-25).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mino et al. in view of Childers et al. as applied to claim 14 above, and further in view of Roskowski et al. (US 5,269,003). The teachings of Mino et al. modified by Childers et al. have been discussed above.

As to claim 15, Mino et al. modified by Childers et al. fails to disclose a first multiplexer for selecting one of a first one of the plurality of pixels and a second one of the plurality of pixels; a second multiplexer for selecting another of the first one of the plurality of pixels and the second one of the plurality of pixels, from the first multiplexer; a third multiplexer for selecting one of a third one of the plurality of pixels and a fourth one of the plurality of pixels; a fourth multiplexer for selecting another of the third one of the plurality of pixels and the fourth one of the plurality of pixels, from the third multiplexer; a fifth multiplexer for multiplexing outputs from the first multiplexer, the second multiplexer, the third multiplexer, and fourth multiplexer; and the selections of the first multiplexer, the second multiplexer, the third multiplexer, and the fourth multiplexer being controlled by the indicator provided by the state machine.

Roskowski et al. teaches a first multiplexer (FIG. 3, "multiplexor 27") for selecting one of a first one of the plurality of pixels and a second one of the plurality of pixels; a second multiplexer (FIG. 3, "multiplexor 28") for selecting another of the first one of the plurality of pixels and the second one of the plurality of pixels, from the first multiplexer; a third multiplexer (FIG. 3, "multiplexor 29") for selecting one of a third one of the plurality of pixels and a fourth one of the plurality of pixels; a fourth multiplexer (FIG. 3,

"multiplexor 30") for selecting another of the third one of the plurality of pixels and the fourth one of the plurality of pixels, from the third multiplexer (Col. 5 line 58 through Col. 6 line 7); a fifth multiplexer (FIG. 3, "accumulator circuit 42") for multiplexing outputs from the first multiplexer, the second multiplexer, the third multiplexer, and fourth multiplexer; and the selections of the first multiplexer, the second multiplexer, the third multiplexer, and the fourth multiplexer being controlled by the indicator provided by the state machine (FIG. 3, "decoder 25", Col. 6 lines 46-67).

Therefore, in view of Roskowski et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Mino et al. and Childers et al. by incorporating the plurality of multiplexors, the accumulator circuit and the decoder to write in order the pixels being transferred in order to reduce the cost of computer systems, increase the performance of the system and wasting no memory space (Col. 2 lines 5-17).

10. Claims 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mino et al. in view of Childers et al. as applied to claim 16 above, and further in view of Baden et al. (US 5,640,545). The teachings of Mino et al. modified by Childers et al. have been discussed above.

As to claim 20, Mino et al. modified by Childers et al. fails to disclose rearranging the plurality of pixels in plurality of different pixel orders; receiving an indicator indicating the pixel order; and selecting the pixels rearranged in one of the plurality of different pixel orders based on the indicator indicating the pixel order.

Baden et al. teaches rearranging the plurality of pixels in plurality of different pixel orders ("pixel swaps", Col. 15 lines 39-55); receiving an indicator (FIG. 6, "BE MODE/LE MODE* control signal **655**") indicating the pixel order (Col. 16 lines 35-43); and selecting the pixels rearranged in one of the plurality of different pixel orders based on the indicator indicating the pixel order (output of the swap multiplexor **651** of FIG. 6, Col. 16 lines 35-65).

Therefore, in view of Baden et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Mino et al. and Childers et al. by incorporating the method steps of swapping the pixel order based on the Bid Endian/Little Endian Mode control signal and selecting the rearranged pixels in order to implement it on a compact hardware configuration and eliminating the need for hardware dedicated system to perform a conditional conversion algorithm (Col. 18 lines 16-25).

As to claim 26, as understood, Mino et al. modified by Childers et al. fails to disclose a demultiplexer for separating the plurality of pixels; a plurality of multiplexers for combining the separated plurality of pixels in a corresponding plurality of pixel orders; and another multiplexer for selecting an output from one of the plurality of multiplexers, based on an indicator indicating the pixel order provided by the state machine.

Baden et al. teaches a demultiplexer for separating the plurality of pixels (FIG. 5, "expansion bus **329**", Col. 6 lines 43-56); a plurality of multiplexers for combining the

separated plurality of pixels in a corresponding plurality of pixel orders (FIG. 5, "pixel swaps **513, 515** and second pass-through **517**", Col. 15 lines 18-34); and another multiplexer for selecting an output from one of the plurality of multiplexers, based on an indicator (FIG. 5, "pixel depth **511**") indicating the pixel order provided by the state machine (FIG. 5, "block 501", Col. 13 line 64 through Col. 15 line 38).

Therefore, in view of Baden et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Mino et al. and Childers et al. by incorporating the expansion bus to receive the pixels in a separated manner, using the pixel swaps and pass-through based on the pixel depth signal to combine the pixel order in a plurality of ways and providing its output in the predetermined order as specified by the control signal in order to provide a mechanism in a frame buffer controller for detecting when the endian-ness of a frame buffer access request is incompatible with the physical storage format of the frame buffer, and for correctly making the necessary pixel conversions (Col. 3 lines 39-43).

11. Claims 27-31, 33, 35, and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mino et al. in view of Baker et al. (US 5,777,601).

As to claims 27 and 38, Mino et al. teaches a method/system for displaying frames (Col. 6 lines 49-51), said method comprising: fetching (a first circuit for fetching) a portion of a frame stored in a frame buffer (FIG. 1, "frame buffer region **22** and data transfer", Col. 6 line 47 through Col. 7 line 8); storing (a buffer for storing) the portion of the frame in another buffer (FIG. 1, "data buffer **11**", Col. 6 lines 12-19); fetching (a state

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machine for fetching) a plurality of pixels from the portion of the frame (FIG. 1, "data processor **9**", Col. 15 lines 11-25).

However, Mino et al. fails to disclose storing (a luma pixel register for storing) luma pixels in a luma pixel register, if the plurality of pixels comprise luma pixels; and storing (a chroma pixel register for storing) chroma pixels in a chroma pixel register, if the plurality of pixels comprise chroma pixels.

Baker et al. teaches storing (a luma pixel register for storing) luma pixels in a luma pixel register (FIG. 4, "register **410**"), if the plurality of pixels comprise luma pixels (Col. 16 lines 47-50); and storing (a chroma pixel register for storing) chroma pixels in a chroma pixel register (FIG. 4, "registers **400** and **402**"), if the plurality of pixels comprise chroma pixels (Col. 14 lines 57-66).

Therefore, in view of Baker et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mino et al.'s method/system by incorporating the method steps and registers for storing luma pixels in a luma pixel register, if the plurality of pixels comprise luma pixels; and storing chroma pixels in a chroma pixel register, if the plurality of pixels comprise chroma pixels in order to require a simple hardware configuration to generate video signals such as video control information (Col. 3 lines 47-54).

As to claims 28 and 39, Mino et al. further teaches decoding (a video decoder for decoding) the frame (FIG. 1, "address decoder **12**", Col. 5 lines 47-64 and Col. 6 lines

12-19); and storing the frame in the frame buffer (FIG. 1, “main memory 2”, Col. 6 line 14-19 and FIG. 9B, Col. 9 lines 19-23).

As to claims 29, 30, 40 and 41, Mino et al. further teaches the another buffer forms a portion of a display engine (FIG. 1, “interface section 10) and a pixel feeder (FIG. 1, “transfer parameter generator 14”, Col. 5 lines 38-46).

As to claim 31, Mino et al. fails to disclose receiving the plurality of pixels; and providing the luma pixels to the luma pixel register, if the plurality of pixels comprise luma pixels.

Baker et al. further teaches receiving the plurality of pixels (FIG. 4, “Hbus 202”, Col. 15 lines 14-18); and providing the luma pixels to the luma pixel register, if the plurality of pixels comprise luma pixels (FIG. 4, “register 410”, Col. 16 lines 47-50).

As to claim 33, Mino et al. fails to disclose receiving the plurality of pixels; and providing the chroma pixels to the chroma pixel register, if the plurality of pixels comprise chroma pixels.

Baker et al. further teaches receiving the plurality of pixels (FIG. 4, “Hbus 202”, Col. 15 lines 14-18); and providing the chroma pixels to the chroma pixel register, if the plurality of pixels comprise chroma pixels (FIG. 4, “registers 400 and 402”, Col. 14 lines 57-66).

As to claim 35, Mino et al. fails to disclose receiving the plurality of pixels; providing chroma Cr pixels to a chroma Cr pixel register, if the plurality of pixels comprise chroma Cr pixels; and providing chroma Cb pixels to a chroma Cb pixel register, if the plurality of pixels comprise chroma Cb pixels.

Baker et al. further teaches receiving the plurality of pixels (FIG. 4, "Hbus **202**", Col. 15 lines 14-18); providing chroma Cr pixels to a chroma Cr pixel register (FIG. 4, "register **400**"), if the plurality of pixels comprise chroma Cr pixels; and providing chroma Cb pixels to a chroma Cb pixel register (FIG. 4, "register **402**"), if the plurality of pixels comprise chroma Cb pixels (Col. 11 lines 49-62 and Col. 14 lines 57-66).

12. Claims 32, 34 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Mino et al. in view of Baker et al. as applied to claim 27 above, and further in view of Canfield (US 6,501,507). The teachings of Mino et al. modified by Baker et al. have been discussed above.

As to claims 32, 34 and 36, Mino et al. modified by Baker et al. fails to disclose receiving the plurality of pixels over a first path; receiving a portion of the plurality of pixels over a second path; selecting the plurality of pixels from the first path, if all of the plurality of pixels are luma/chroma pixels; and selecting the portion of the plurality of pixels from the second, if a portion of the plurality of pixels are luma/chroma pixels and another portion of the plurality of pixels are chroma/luma pixels.

Canfield teaches receiving the plurality of pixels over a first path (FIG. 2, "LUMA/CHROMA FROM MEMORY paths respectively"); receiving a portion of the

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plurality of pixels over a second path (FIG. 2, "input of MUX 30"); selecting the plurality of pixels from the first path, if all of the plurality of pixels are luma/chroma pixels (FIG. 2, "input of MUX's 35 and 36 respectively); and selecting the portion of the plurality of pixels from the second, if a portion of the plurality of pixels are luma/chroma pixels and another portion of the plurality of pixels are chroma/luma pixels (FIG. 2, "Selection of MUX 30", Col. 3 lines 7-29).

Therefore, in view of Canfield, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Mino et al. and Baker et al. by incorporating the multiplexors as shown in FIG. 2, and properly selecting the desired path when luma/chroma pixels are being proportioned, if they correspond only to luma/chroma pixels or selecting another path if there is portions corresponding to luma and chroma pixels in order to support different video image resolutions, as it is the case of MPEG format (Col. 3 lines 7-29).

Allowable Subject Matter

13. Claims 37, 42 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
14. The following is a statement of reasons for the indication of allowable subject matter: The closest prior art made of record fails to disclose the feature of storing at least one of the pixels from the portion of the plurality of pixels from the second path in the chroma Cr/Cb pixel register, if the portion of the plurality of pixels are selected, as

recited in claim 37, and the multiplexer configuration recited in claims 42 and 43 for the reception of the portions of the plurality of pixels and the selection made by the state machine when the pixels comprises both luma and chroma pixels.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bixby et al. disclose a MPEG Dual-Channel Decoder Data and Control Protocols for Real-Time Video Streaming, Jun disclose a Device and Method of Converting Scanning Pattern of Display Device, Saxena et al. disclose a Method and Apparatus for Improving Processor to Graphics Device Local Memory Performance, and Schultz et al. disclose Formatting of Recompressed Data in an MPEG Decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose M. Torres whose telephone number is 571-270-1356. The examiner can normally be reached on Monday thru Friday: 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on 571-272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JMT
03/13/2007

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SUPERVISORY PATENT EXAMINER